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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,884	04/12/2001	Steve M. Danziger	L/M-102-DIV	2718

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EXAMINER	
PERT, EVAN T	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/832,884	DANZIGER ET AL.	
	Examiner	Art Unit	
	Evan T. Pert	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on June 4, 2001. These drawings are approved.

Claim Objections

2. Dependent claims 2, 3, 4, 5 and 8 are objected to for informalities:

Claim 2 (Objection)

The phrase "wire bond pad" does not match the linguistic phrase "wire bond connections" recited in antecedent claim 1, but the two phrases are interpreted conceptually as being equivalent (i.e. both phrases represent inherently plural "wire bond pad connections"), for purposes of examination.

Claim 3 (Objection)

The phrase "wire bond pad connections" does not match the linguistic phrase "wire bond connections" recited in antecedent claim 1, but both phrases are understood to be equivalent (i.e. both are "wire bond pad connections"), for purposes of examination.

The phrase "solder ball array contacts" does not match the linguistic phrase "solder ball array connections" recited in antecedent claim 1, but both phrases are understood as being equivalent (i.e. both are "solder ball array contact connections"), for purposes of examination.

Claim 4 (Objection)

The phrase "wire bond pads" does not match the linguistic phrase "wire bond connections" recited in antecedent claim 1, but both phrases are understood to be equivalent (i.e. both are "wire bond pad connections"), for purposes of examination.

Claim 5 (Objection)

The phrase "solder ball array" does not match the linguistic phrase "solder ball array connections" recited in antecedent claim 1, but both phrases are understood as being equivalent (i.e. both are "solder ball array connections"), for purposes of examination.

The phrase "wire bond pads" does not match the linguistic phrase "wire bond connections" recited in antecedent claim 1, but both phrases are understood as being equivalent (i.e. both are "wire bond pad connections"), for purposes of examination.

The phrase "integrated circuit" does not match the linguistic phrase "integrated circuit device", but both are understood as being equivalent (i.e. both are an "integrated circuit chip or die" (which may be packaged, partially packaged, or completely packaged).

A period (.) is missing after "testing" at the end of the claim.

Claim 8 (Objection)

To match antecedent language recited in claim 1, after the first occurrence of "solder ball array", insert --forming the solder ball array connections--, which has been assumed for purposes of examination.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 - Claim 2 recites the limitation "stress tolerant solder ball connections" at lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Claims 2 and 8 - The term "stress tolerant" with respect to the recited "solder ball array" (inherent to the solder ball array "connections") in claims 2 and 8 is a relative term which renders the claims indefinite. The term "stress *tolerant*" is not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably aware of the scope of the invention.

Applicant *does* seem to suggest that a "stress tolerant" array *could* include an ordinary grid of ball bumps in a BGA wherein at least some bumps are located at the center of a grid and not just at an outer periphery [page 6, lines 1-3]. However, no definitive quantitative/qualitative criterion is set forth by applicant's disclosure, for one of ordinary skill in the art to ascertain the scope of meaning of "stress tolerant" with regard to the bumps of a BGA.

For purposes of examination, in view of applicant's disclosure, all BGA (Ball Grid Array) connections are interpreted as being inherently "stress tolerant" whenever the concept of BGA stress is addressed; otherwise the BGA connections would fail at the slightest immeasurable stress from the slightest gradient of forces on the connections. One could even reasonably say that all BGA connections have experienced some level of "stress" ever since the day they were first conceived, so they must all inherently be "stress tolerant" (to *some* degree) to operate functionally as intended.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi (JP 10-135281).

Claim 1 - Takahashi teaches "a known good integrated circuit device" (cover figure in view of paragraph [0018]) having "optional solder ball array or wire bond connections" (wherein "optional" is an "intended use" bearing little patentable weight, yet wire bond pad connections 22 are reasonably "optional" since the integrated circuit device 1 could undergo testing and operation using only the BGA 23); solder ball array 23 on device 1 surface; and wire bond

connections 22 electrically connected to the solder ball array connections 23 [abstract].

Regarding the "product-by-process" limitations of the last 8 lines of claim 1, applicant is reminded that "process limitations" bear little patentable weight unless some observable and distinguishable structure necessarily results from adhering to the process limitations [See MPEP 2113]. In the instant case, it is not clear how one could tell if the device was tested or not since testing does *not necessarily* cause discernable damage, and both BGA connections 23 and wire bond connections 22 are "available for connection" since both types of electrical connections remain as part of the final package and are externally accessible on the package [abstract + Fig. 3].

Claim 2 - While bearing little patentable weight as a "product-by-process" claim, a primary intent of Takahashi's invention is to avoid damaging the BGA during KGD testing by using wire bond connections 22 for testing to leave the BGA for actual use "protected from abrasion and damage" [last sentence of abstract]. Further, the BGA of Takahashi is inherently "stress tolerant", at least to some degree because it is a grid (see paragraph [003]) and results in a KGD (see paragraph [0018]).

Claims 3 & 4 - Both BGA connections 23 and wire bond connections 22 are "on the same side of integrated circuit device 1" and are also "on substantially the same level of the integrated circuit device 1" [cover figure].

Claim 5 - The final CSP (chip scale package) includes both the BGA connections 23 and the wire bond connections 22 (e.g. see paragraph [0018] with Fig. 3).

Claim 6 - The "connections 23" are *wire bond* connections, and are therefore inherently bonded *metallurgical* connections.

Claim 8 - In view of the indefiniteness of "stress tolerant" set forth above, Takahashi's BGA is reasonably interpreted as being inherently "stress tolerant" to some degree.

Claim 9 - The integrated circuit device is a "die (chip) 1".

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi as applied to claim 1 above, and further in view of L.S. Goldman (1972 article).

Takahashi does not disclose that the BGA 23 is of a type for controlled collapse chip connections.

Goldman teaches that "one of the most significant advantages of using controlled (chip) collapse (connections) is "the ability to correct misregistration" [text beginning under Fig. 1 at left column of page 332].

It would have been obvious to one of ordinary skill in this art to adopt C4 as the method for connecting the BGA 23, making the BGA "controlled collapse chip connections" when mounted for intended use. One of ordinary skill in the art would have been motivated by a desire to "correct misregistration" when the BGA bumps melt and bond to the final mounting [as taught by Goldman].

7. Claims 2 and 8 were rejected under 35 U.S.C. 102(b) as anticipated by Takahashi (since "stress tolerant" is deemed inherent to Takahashi's BGA 23 (in view of the rejections of claims 2 and 8 under 35 USC 112, 2nd paragraph as set forth above). In the alternative, claims 2 and 8 are rejected under 35 U.S.C. 103(a) as obvious over Takahashi as applied to claim 1, and further in view of L.S. Goldman (1969 article).

Takahashi is silent regarding the concept of "stress tolerant" BGA connections.

Goldman teaches, in 1969, that controlled collapse connections are subject to thermal "shear stress" cycling which can cause device failure, and that "it is important to design...to minimize the likelihood of failure" which is an equivalent form of language stating that the connections, which are subject to shear stress from thermal expansion and contraction, are advantageously "stress tolerant".

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to make the connections of BGA 23 in Takahashi "stress tolerant".

One of ordinary skill in the art would have been motivated to make the BGA "stress tolerant" by a desire to avoid the readily apparent problem of device failure from failed electrical connections resulting from thermal stress [text of Goldman bridging pages 251 and 252].

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi. While Takahashi et al. is seemingly silent regarding connection to "an *end* use device", this concept is readily grasped as the whole point of making a KGD CSP integrated circuit device in the first place [See MPEP 2144.04 - Implicit Disclosure]. What would be the purpose of only making integrated circuit chip products that are n*ever* connected in an end use product?

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to connect the BGA of Takahashi to an end use device, after testing using wire bond connections 22 [abstract's last sentence in view of "Implicit Disclosure"]. One of ordinary skill in the art would have been motivated to "connect to an end use device" to make a functional product that can be sold for profit.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan T. Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 703-308-1680. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ETP
September 19, 2002

EVAN PERT